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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD.,

Plaintiff,

vs.

AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL CORP., MATROX TECH, INC., AND AEROFLEX COLORADO SPRINGS, INC.

Defendants.

SYNOPSYS, INC.,

Plaintiff,

vs.

RICOH COMPANY, LTD.,

Defendant.

Case No. C03-04669 MJJ (EMC)

Case No. C03-02289 MJJ (EMC)

NOTICE OF MOTION AND MOTION FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT (HARDWARE CELLS)

[SUMMARY JUDGMENT MOTION NO. 2]

Date: September 26, 2006
Time: 9:30 a.m.
Courtroom: 11, 19th Floor
Judge: Martin J. Jenkins

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NOTICE OF MOTION AND MOTION

PLEASE TAKE NOTICE that on September 26, 2006, at 9:30 a.m., before the Honorable Martin J. Jenkins in Courtroom 11, 19th Floor, in the United States District Court, 450 Golden Gate Avenue, San Francisco, California, Plaintiff Synopsys, Inc. ("Synopsys") and Defendants Aeroflex Incorporated, Aeroflex Colorado Springs, Inc., AMI Semiconductor, Inc., Matrox Electronic Systems Ltd., Matrox Graphics Inc., Matrox International Corp., and Matrox Tech, Inc. ("the Customer Defendants") will move for summary judgment pursuant to Rule 56 of the Federal Rules of Civil Procedure that the Customer Defendants do not infringe claims 13-17 of U.S. Patent No. 4,922,432 ("the '432 patent"). This motion is based on the memorandum of points and authorities set forth below, the accompanying declarations, exhibits, and proposed order, the oral arguments of counsel at the hearing on this motion, and all other pleadings and matters of record in these actions.

MEMORANDUM OF POINTS AND AUTHORITIES

I. INTRODUCTION

Synopsys and the Customer Defendants move for summary judgment that the Design Compiler system does not have stored data describing hardware cells and does not select hardware cells as required by element B and F of claim 13 of United States Patent 4,922,432.

The Court's claim construction of the final element, element F, of Claim 13 requires that the accused system "map[] the specified stored function to a corresponding stored hardware cell." Ex. 8 at 20. The fundamental question at issue in this motion is what is a "hardware cell." Synopsys and the Customer Defendants contend that the claim construction is quite clear, consistent with the plain meaning of the claim language as well as all of the intrinsic evidence, that a "hardware cell" must be something that maps to or corresponds to a specified function. Thus, if the specified function to be performed is "add," then the hardware cell to which it must be mapped is something that can perform the function of adding, such as an adder.

Moreover, the claim goes on to say how the hardware cells must be selected. The claim says that cells must be selected by "applying rules" to the "specified stored function." Synopsys and the Customer Defendants interpret this consistent with its plain language to mean that whatever Ricoh

contends are "rules" must be applied to whatever Ricoh contends are "specified stored functions" to select the cells. Finally the claim requires that the hardware cells be selected using "cell selection rules," which is also clear on its face.

Because Ricoh cannot read the plain language of the claim onto the Design Compiler system, as will be explained in more detail below, Ricoh simply re-writes the claims so they will read on the Design Compiler system. This, however, is a literal infringement case, and Ricoh must find each element of the asserted claims ***explicitly*** as stated in the Design Compiler system. This is not a close call – Ricoh simply cannot read claim 13 onto the Design Compiler System. Because it cannot do so, summary judgment in favor of Synopsys and the Customer Defendants must be granted.

II. FACTS

A. Background

Ricoh alleges that the Customer Defendants infringe claims 13-17 of the '432 patent by creating designs for application specific integrated circuits ("ASICs") using Synopsys' Design Compiler system. The '432 patent relates generally to a computer-aided design ("CAD") system for ASIC design in which a user inputs a description of the desired operations for the ASIC into the CAD system. The output of the system, after a series of steps, is a "netlist" defining the hardware cells which are needed to perform the desired function of the integrated circuit. Ricoh has asserted that the Customer Defendants infringe claims 13-17 of the '432 patent under a theory of literal infringement, as

opposed to infringement under the doctrine of equivalents.[1] *See* Ex. 2 3-6 at 25:25-27.[2]

Claim 13 of the '432 patent is the *only* independent claim asserted by Ricoh.[3] Thus, if even one element of claim 13 is found not to be met, this case is over. The text of Claim 13 reads:

> A computer-aided design process for designing an application specific integrated circuit which will perform a desired function comprising:
>
> [A] storing a set of definitions of architecture independent actions and conditions;
>
> [B] storing data describing a set of available integrated circuit hardware cells for performing the actions and conditions defined in the stored set;
>
> [C] storing in an expert system knowledge base a set of rules for selecting hardware cells to perform the actions and conditions;
>
> [D] describing for a proposed application specific integrated circuit a series of architecture independent actions conditions;
>
> [E] specifying for each described action and condition of the series one of said stored definitions which corresponds to the desired action or condition to be performed; and
>
> [F] selecting from said stored data for each of the specified definitions a corresponding integrated circuit hardware cell for performing the desired function of the application specific integrated circuit, said step of selecting a hardware cell comprising applying to the specified definition of the action or condition to be performed, a set of cell selection rules stored in said expert system knowledge base and generating for the selected integrated circuit hardware cells, a netlist defining the hardware cells which are needed to perform the desired function of the integrated circuit and the interconnection requirements therefor.[4]

Generally, claim 13 requires that three sets of data be stored in a CAD system: (1) a set of "definitions of architecture independent actions and conditions" (element A); (2) data describing "hardware cells" for performing those actions and conditions (element B); and (3) a set of "rules" for selecting the

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[1] None of Ricoh's experts alleges that the Customer Defendants infringe the '432 patent under the doctrine of equivalents, nor is there any such allegation in Ricoh's Final Infringement Contentions under Patent L.R. 3-6.

[2] Unless otherwise noted, all exhibits referenced in this motion are attached to the Declaration of Denise M. De Mory In Support of Synopsys' and Customer Defendants' Summary Judgment Motions filed concurrently herewith. All deposition references are likewise included in the De Mory Declaration.

[3] Claims 14-17 are all dependent on claim 13.

[4] The elements of claim 13 have been designated by letter for easy reference.

hardware cells to perform the actions and conditions (element C). Once these three sets of data have been stored, a user describes a series of "architecture independent actions and conditions" that the user wants to include in the desired ASIC (element D). The CAD system then takes that user description and specifies a definition from the set of definitions stored in element A. The CAD system then applies the selection rules from element C to each specified definition of element E to "select" from the stored data describing the hardware cells (element B), a hardware cell that corresponds to the specified architecture independent action or condition. The system then generates a netlist defining the hardware cells which are needed to perform the desired function of the integrated circuit.

From the viewpoint of the user, the user must first input "architecture independent actions and conditions" into the accused system.[5] The Court interpreted this step to require "describing an input specification containing a series of desired functions to be performed by the desired ASIC." The system must specify a "stored definition" for each architecture independent action and condition, or in the Court's terms, for each architecture independent function. Ex. 8 at 14. The specified definition is later referred to by the Court as a "specified stored function." The system must then select a hardware cell corresponding to the specified stored function. Indeed, the Court interpreted "selecting from said stored data for each of the specified definitions a corresponding integrated circuit hardware cell" as "mapping the specified stored function to a corresponding stored hardware cell." Ex. 8 at 20. Finally, the selection must occur by applying "rules" to the specified definitions, i.e., the specified stored functions. Indeed, the Court ruled that selection must occur by "mapping of the specified definitions [described above as specified stored functions] to the stored hardware cell descriptions by applying to the specified definitions a set of cell selection rules." Ex. 8 at 21.

Synopsys and the Customer Defendants contend, as set forth below, that the plain language of the claims as well as the Court's claim construction is clear, and that Ricoh's infringement theory fails as a matter of law.

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[5] The Court defined "architecture independent actions and conditions" as functional or behavioral aspects of a portion of a circuit (or circuit segment) that does not imply a set architecture, structure, or implementing technology, but excludes the use of register-transfer level descriptions as taught in Darringer. Ex. 8 at 12.

B. Ricoh's Infringement Theory Is Premised On A Faulty Reading Of the Plain Language Of the Claims

Ricoh's entire infringement theory is premised on its claim that the "hardware cells" described in element B and F must be primitive logic gates, such as ANDs and ORs. Ricoh asserts this, of course, solely because the Target Technology libraries used by the Customer Defendants only contain primitive logic gates, and without regard to the meaning of the claims. The plain meaning of the claims, as interpreted by the Court, and supported by the intrinsic evidence, however, is that "hardware cells" are not ANDs and ORs. Instead, "hardware cells", as described in detail below, are functional circuit components (whose logic function requires the use of more than one primitive gate) that can be mapped or correspond to specified stored functions/definitions.

There is also a final question with regard to the types of information required to be stored for each hardware cell. Ricoh quite conveniently takes one position for infringement purposes and another for invalidity. The alleged cells stored in Design Compiler do not contain the level of detail Ricoh maintains the claim requires for purposes of its invalidity analysis.

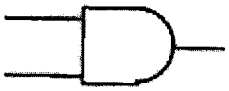
C. The Plain Language of the Claim Is Clear: Hardware Cells Are Not Primitive Logic Gates, But Are Instead Circuit Components (Whose Logic Function Requires The Use Of More Than One Primitive Gate) That Map Or Correspond To Specified Functions To Be Performed By The Described ASIC

Turning to the plain language of the claim, it becomes abundantly clear that Ricoh's reading of the claim to try to fit the round peg of Design Compiler into the square hole of the claims of the '432 patent must be rejected. Element F is the step of selecting for "*each* specified definition" in element E "*a hardware cell*" from the data stored in element B for performing the desired (specified) function: "selecting from *said stored data* for each of the specified definitions *a corresponding integrated circuit hardware cell* for performing the desired function of the application specific integrated circuit."

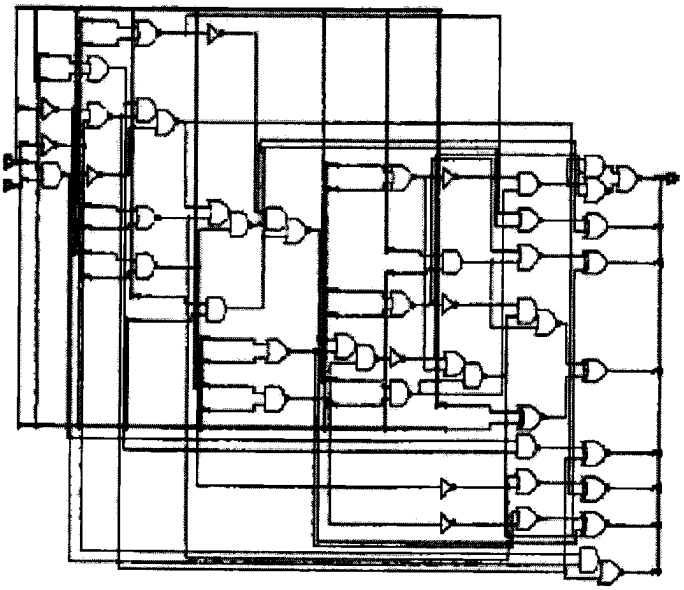
The plain language of the claim requires selecting from said stored data (element B) for EACH specified definition A (i.e., ONE) corresponding integrated circuit hardware cell. Moreover, the cell must perform the desired function. And, as noted above, the Court interpreted this language as: "mapping the specified stored function to a corresponding stored hardware cell." Ex. 8 at 20:13-15. Thus, it is very clear from the plain language of the claim as well as the Court's interpretation that for each specified definition, or in the words of the Court's claim construction, "specified stored function," there must be "a corresponding stored hardware cell" in the cell library that performs the specified function. Thus, the "hardware cells" of element B and F are not primitive logic gates such as ANDs, ORs, or NORs, but rather circuit components (i.e., implementations), such as adders, subtractors, and multipliers, that for example, carry out an add, subtract, or multiply functions and are comprised of many logic gates.

For purposes of illustrating the differences, it may be helpful to look at the details of a primitive logic gate, such as AND, versus an adder, such as a ripple carry adder, or in contrast, a carry look ahead adder.

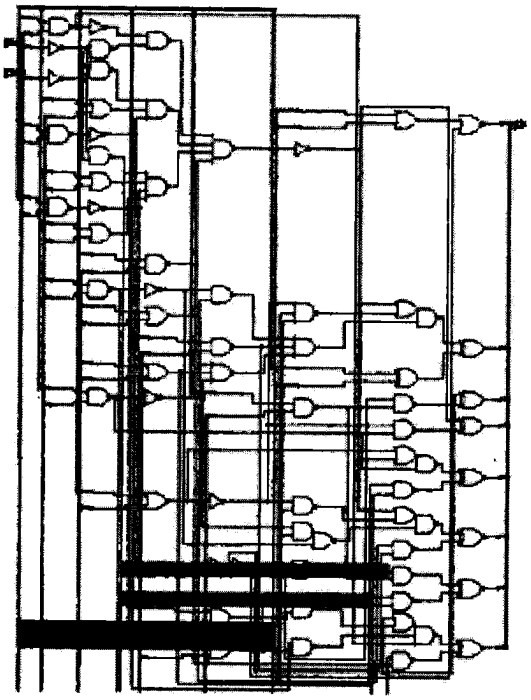
An AND gate is depicted as follows:



In contrast, an exemplary adder implementation called a ripple carry adder, that can, among other possible implementations, correspond to a specified ADD function, can be depicted at the gate level as follows:



An alternative exemplary adder implementation, called a carry look ahead adder, could also be selected as corresponding to an ADD function and can be depicted at the gate level as follows:



The ripple carry or carry look ahead adders depicted above correspond to a function, ADD, while the AND gate (pursuant to Ricoh's infringement theory) does not.

The intrinsic evidence is fully consistent with this interpretation. Indeed, the description of the cell library in the specification confirms the claims' plain meaning that the cell must correspond to a function, such as ADD, and not be just a primitive logic gate. The specification provides that the cell library contains four types of information for each cell:

(1) functional level information: description of the cell at the RTL level.

(2) logic level information: descriptions in terms of gates and flip-flops.

(3) circuit level information: description at the transistor level.

(4) layout level information: geometrical mask level specification.

Col. 9:21-34. In addition, for each cell, there are certain attributes that aid the rules in cell selection. Col. 9:35-50.

Storing this information for a cell makes sense if the cell is an adder corresponding to ADD, but makes no sense if the cell is simply a primitive gate as depicted above. If the cells were simply AND or OR gates, there would be no need to store both (1) and (2), because the function and the logic would be the same. An OR gate is comprised of an OR gate and performs and OR function. Moreover, it would not make sense to say that the logic level information should be described in terms of "gates and flip-flops," since a single gate is *all* that could exist here. In contrast, it makes perfect sense to describe an implementation of a circuit element, such as an adder, in terms of "gates and flip-flops" *and* to specify the functional description (add) separate[6] and apart from the logic description. Thus, the specification makes clear that the cells are not simple or primitive logic gates.

An example from the specification is illustrative. The Court may recall that that the "specified definitions" of stored functions in the patent were macros, including for example, ADD (A, B, C). See Col. 7 at Table 1. In the example set out in the patent, during the selecting step: "The addition macro ADD(A,B,C) results in the generation of a register for each of the input values, A and B, and a register

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[6] The fact that the cell library includes a description of the functional level information at a register transfer level suggests, in fact, that the cells are more than just implementations. It suggests instead, that the cells are specified in terms of not only an implementation corresponding to the function, but also the needed register and control information to actually implement the function as a block in the circuit, given that the input is purely architecture independent.

for the output value C, and in the generation of an adder block." Col. 13:43:-47. As decribed in the specification, the cell selector then selects "an optimum cell for a block." Col. 9:22-23. Thus, an "adder" cell is selected for an "adder" block from among all of the "adder" cells, (i.e., different implementations) in the cell library. The selected cell cannot be just an AND or OR gate, but rather a more complex structure.

D. Cells Must Be Selected By Applying Rules

The plain language of the claim as well as the claim construction clearly requires that the cells be selected using rules. In accordance with the claim language, the cells are selected by applying to the specified stored definition (or stored function) a "set of cell selection rules." The claim says: "said step of selecting a hardware cell comprising applying to the specified definition of the action or condition to be performed" a set of cell selection rules. The Court construed this claim to mean "mapping of the specified definitions [described above as specified stored functions] to the stored hardware cell descriptions by applying to the specified definitions a set of cell selection rules." Thus, in order to infringe, the alleged "rules" must be "applied" to the specified stored definitions to select "a hardware cell" for "each specified definition." These are the words of the claim and the Claim Construction, and they clearly and plainly specify what is required.

E. The Rules Must Be Cell Selection Rules

The claim requires storing a set of rules for selecting hardware cells to perform the actions and conditions. There is nothing ambiguous about this language. The rules must be cell selection rules.

F. Stored Data Must Include Geometrical Information

Now, having identified what a cell is, and how it is selected, the final question is: what is data describing a set of available integrated circuit hardware cells as required by element B. Here, the question is what type of information must be stored for each cell in the library – must one store all four levels of information and all attributes as described in the specification, or does less information satisfy the claims? Synopsys and the Customer Defendants assert that in order for the process described in Claim 13 (and subsequent dependent claims 14-17) each level of information must be stored, and at least some attributes. Because the cells are not simple primitive gates, at a minimum a functional and logic level description must be stored. In addition, because claim 14 requires the mask data of element

(4) above, the mask data may be required. Synopsys and the Customer Defendants do not seek to read limitations from the specification into the claim, and thus, do not assert all these elements of the cell library described in the specification must be stored for each element. What is clear, however, is that the claims must be interpreted consistently for infringement purposes as well as for validity purposes. Because Ricoh claims for purposes of its invalidity analysis that "geometric data" regarding the cells, i.e., "(4) layout level information: geometrical mask level specification," then "geometric data" is also required to infringe the claims. For purposes of avoiding anticipation by VEXED, an asserted piece of prior art, Dr. Soderman distinguishes VEXED by saying "There is no technology specific library of 'hardware cells' composed of geometrical information of hardware components (e.g., NAND, NOR gates, etc.) from which to build an ASIC." Soderman Rebuttal Report at 8. Thus, in order to infringe, the "geometrical information" must likewise be stored for the accused system.

G. There Is No Dispute That the Alleged Rules In The Design Compiler System Are Not Used To Select Cells

[7] Synthetic operators are internal to the Design Compiler system.

[8] Synthetic module selection is an intermediate step within Design Compiler that is not significant for purposes of this analysis.

III. ARGUMENT

A. Legal Standard

Summary judgment is proper "if the pleadings, depositions, answers to interrogatories and admissions on file, together with the affidavits, if any, show that there is no genuine issue as to any

material fact and that the moving party is entitled to a judgment as a matter of law." Fed. R. Civ. P. 56(c). In the context of a patent case, this means that an accused infringer seeking summary judgment of non-infringement may meet its initial responsibility either by providing evidence that would preclude a finding of infringement, or by showing that the evidence on file fails to establish a material issue of fact essential to the patentee's case. *See Novartis Corp. v. Ben Venue*, 271 F.3d 1043, 1046, 1050-51, 1055 (Fed. Cir. 2001). Once the moving party makes this initial showing, the burden shifts to the non-moving party to "designate specific facts showing that there is a genuine issue for trial." *Celotex Corp. v. Catrett*, 477 U.S. 317, 324 (1986) (citation omitted); *Aguilera v. Pirelli Armstrong Tire Corp.*, 223 F.3d 1010, 1019 (9th Cir. 2000) (citation omitted) ("On a motion for summary judgment, the non-moving party cannot simply rest on its allegations without any significant probative evidence tending to support the complaint").

Determining whether a patent claim has been infringed involves two steps: (1) claim construction to determine the scope of the claims, followed by (2) determination of whether the properly construed claim encompasses the accused devices. *Vitronics v. Conceptronic, Inc.*, 90 F.3d 1576, 1581-82 (Fed. Cir. 1996). Literal infringement requires that the patentee prove that the accused product or process meets every element or limitation of a claim. *Rohm and Haas Co. v. Brotech Corp.*, 127 F.3d 1089, 1092 (Fed. Cir. 1997). If even one element or limitation is missing or is not met as claimed, then there is no literal infringement. *See Mas-Hamilton Group v. LaGard, Inc.*, 156 F.3d 1206, 1211 (Fed. Cir. 1998); *see also Lantech, Inc. v. Keip Mach. Co.*, 32 F.3d 542, 547 (Fed. Cir. 1994) ("For literal infringement, each limitation of the claim must be met by the accused device exactly, any deviation from the claim precluding a finding of infringement."). Summary judgment of no literal infringement is appropriate when no reasonable jury could find every limitation recited in an asserted claim is found exactly in the accused device. *See Johnston v. IVAC Corp.*, 885 F.2d 1574, 1576-80 (Fed. Cir. 1989).

B. The Use Of The Design Compiler System Does Not Infringe.

C. If Claim 13 Is Not Infringed, then Claims 14-17 Cannot Be Infringed.

Claims 14-17 are all dependent on claim 13. ['432 patent, col. 16:14-17:10]. Thus, if the Court finds that claim 13 is not infringed, then claims 14-17 also are not infringed. *See Wahpeton Canvas Co., Inc. v. Frontier, Inc.*, 870 F.2d 1546, 1552 n.9 (Fed. Cir. 1989) ("One who does not infringe an independent claim cannot infringe a claim dependent on (and thus containing all the limitations of) that claim.").

IV. CONCLUSION

Based on the Court's interpretation of the plain meaning of the claims, the Customer Defendants to not literally infringe, and indeed, the Design Compiler system is not capable of literally infringing, the asserted claims of the '432 patent. The Court should therefore grant summary judgment of non-infringement in favor of the Customer Defendants on all of the asserted '432 patent claims and grant Synopsys, on summary judgment, a declaration that Design Compiler does not infringe the '432.

Dated: August 18, 2006

HOWREY LLP

By: */s/Denise M. De Mory*
Denise M. De Mory
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